REMARKS

Present Status of the Application

Claims 1-13 are pending.

The office action rejected claims 1, 3, 7-9, and 11-13 under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653) in view of Nanba (US 4,665,484) and Fujimoto (US 5,418,913).

The office action rejected claims 2 and 10 under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), Nanba (US 4,665,484) and Fujimoto (US 5,418,913), and further in view of Fried et al (US 5,142,676).

The office action rejected claims 4-6 under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), Nanba (US 4,665,484) and Fujimoto (US 5,418,913), and further in view of Balmer et al (US 5,742,599).

Response to Claim Rejections Under 35 U.S.C. 103(a)

The Office Action dated July 22, 2008 and the Advisory Action dated September 26, 2008 have been received and their contents are carefully considered.

In response to the aforesaid rejections, Applicants have amended claims 1, 2, 3, 4 and 9 to describe the claimed invention more explicitly and to correct several typographical errors. The term "message row that is currently free" is replaced with "target message row". The feature "*the distribution complete flag and the write complete flag of the message target row are both cleared*

without permission of the write control unit and the source controller" is added into independent claim 1, and the feature "*clearing the distribution complete flag and the write complete flag of the target message row without permission of the source controller*" is added into independent claim 9. Such added features are inherently taught in the specification and the drawings of the present application, especially in paragraphs [0006] and [0017] and FIG. 1 that inherently teach that "*the distribution complete flag and the write complete flag of the message row are cleared by the read pointer control unit 170 rather than the write control unit 165 or the source controller 110*". No new matter is introduced.

After entry of said amendments, it is respectfully submitted that the pending claims 1-13 are patentably distinguishable over the cited references for at least the following reasons.

As acknowledged by Examiner's Action, Kawauchi fails to teach the use of a distribution complete flag, as recited by claims 1 and 9. To overcome this admitted deficiency, the Action relies on the teachings of Nanba. However, Applicants believe that the teachings of the references are not sufficient to render the claims 1 and 9 obvious **because the proposed combination of the prior art would change the principle of operation of Nanba**. Please refer to MPEP § 2143.01, subsection VI, which recites "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious". *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). Moreover, Applicants also believe that there is no suggestion or motivation to make the proposed modification **because the proposed modification would render Nanba unsatisfactory for its intended purpose**. Please refer to MPEP § 2143.01,

subsection V, which recites "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification". *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

As recited in claims 1 and 9 of the present application, the distribution complete flag of the target message row is set when the source controller reads an address of the target message row, and the distribution complete flag of the target message row is cleared ***without permission of the source controller*** once the destination controller completes reading the message of the target message row in response to the read request. Referring to FIG. 1 of the present application, a distribution complete flag (C0-C3) of a target message row (130) is set when the source controller (110) reads an address of the target message row (130), and the distribution complete flag (C0-C3) of the target message row (130) is cleared by the read pointer control unit 170 without permission of the source controller 110 once the destination controller (120) completes reading the message of the target message row (130). Therefore, the distribution complete flag (C0-C3) is set in response to the read operation of the source controller (110), and then the distribution complete flag (C0-C3) is cleared in response to the read operation of the destination controller (120), which is different from the source controller (110).

However, Nanba teaches that the lock flag/bit, i.e. the first bit of the GATE, **is set and cleared by the same processor** before the shared resource is released. Firstly, according to the specification of Nanba, the first bit of the GATE is used to indicate whether the shared resource is in a locked status or in an unlocked status. The first bit of the GATE is set to "1" if the shared resource is locked, and the first bit of the GATE is set to "0" if the shared resource is unlocked.

Secondly, Nanba teaches that "*At step 68, the processor P0 applies the address signal indicative of the GATE address via the address bus AB, while applying the data having all bits "1"s to the entire GATE ..... The reason that the all logic "1"s are stored in the entire GATE at step 68, is to prevent the other processors from accessing the shared resource which the processor P0 intends to use*" (see col. 4, line 63 to col. 5, line 7) and that "*a program executed on the processor P0 intends to use a shared resource and hence is going to lock same for the exclusive use thereof*" (see col. 4, lines 41-43). Referring to FIG. 2 of Nanba, when the processor P0 uses a shared resource in the main memory 40, the processor P0 sets all bits of the GATE of the shared resource to "1" so as to prevent the other processors P1 and P2 from using the shared resource. Since the other processors P1 and P2 cannot use the shared resource, which is locked by the processor P0, the first bit of the GATE of the shared resource would not be cleared by the other processors P1 and P2 without the permission of the processor P0. In other words, if Nanba allows the first bit of the GATE being set to "0" (i.e. cleared) without the permission of the processor P0 once the other processor P1 or P2 completes reading data from the shared resource locked by the processor P0, the first bit of the GATE may be set to "0" even if the processor P0 still uses the shared resource. In such case, the processor P0 would fail to lock the shared resource for exclusive use thereof, and the program executed on the processor P0 may operate erroneously due to misplacement or overlap of the shared resource.

For at least the foregoing reasons, the first bit of the GATE of Nanba cannot be cleared in response to the read operation of other processor without the permission of the processor that locks the same shared resource. Otherwise, Nanba will fail to lock the shared resource to prevent other processor from using the shared resource. Therefore, Applicants believe that the teachings of the

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references are not sufficient to render the claims 1 and 9 obvious **since the proposed modification would render Nanba unsatisfactory for its intended purpose and the proposed combination of the prior art would change the principle of operation of Nanba**.

It is respectfully submitted that independent claims 1 and 9 and their dependent claims of the present application are patented over the cited references. Reconsideration and allowance of the application and presently pending claims 1-13 are respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-13 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

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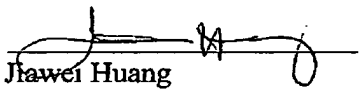

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